

GENERAL DESCRIPTION

The CMT2301 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. ◆

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- -20V/-2.3A , $R_{DS(ON)}$ =130 mΩ@VGS=-4.5V
- -20V/-1.9A , $R_{DS(ON)}$ =190 mΩ@VGS=-2.5V
- ◆ Super high density cell design for extremely low R_{DS(ON)}
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3 package design

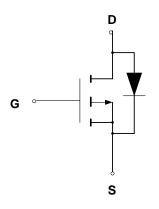
APPLICATIONS

- ◆ Power Management in Notebook
- Portable Equipment
- Battery Powered System
- ♦ DC/DC Converter
- ♦ Load Switch
- ◆ DSC
- ◆ LCD Display inverter

PIN CONFIGURATION

SOT-23-3 Top View 3 NN SONBCE SONBCE 1 2

SYMBOL



P-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT2301M233	SOT-23-3
CMT2301GM233*	SOT-23-3

*Note: G : Suffix for Pb Free Product



ABSOLUTE MAXIMUM RATINGS

Rating			Value	Unit	
Drain- to- Source Voltage		V_{DSS}	-20	V	
Gate-to-Source Voltage		V _{GSS}	±8	V	
Continuous Drain Current(T _J =150°ℂ)	T _A =25°C		-2.5	^	
	T _A =70°C	I _D	-1.5	Α	
Pulsed Drain Current		I _{DM}	-10	Α	
Continuous Source Current(Diode Conduction)		Is	-1.6	Α	
T _A =25℃		<u> </u>	1.25	14/	
Power Dissipation	T _A =70°C	P _D	0.8	W	
Operating Junction Temperature		TJ	150	$^{\circ}\mathbb{C}$	
Storage Temperature Range		T _{STG}	-55/150	$^{\circ}\!\mathbb{C}$	
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	120	°C/W	

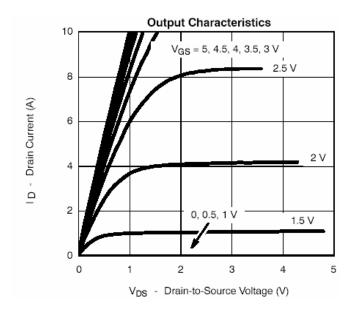
ELECTRICAL CHARACTERISTICS

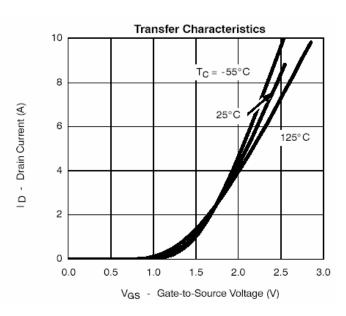
Unless otherwise specified, $T_J = 25^{\circ}C$.

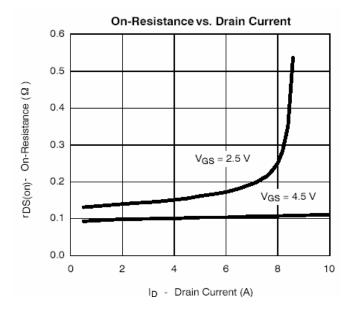
			CMT2301			
Cha	aracteristic	Symbol	Min	Тур	Max	Units
Static						
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	-20			V
$(V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{ A})$		V (BR)DSS				V
Gate Threshold Voltage $(V_{DS} = V_{GS}, I_D = -250 \mu A)$		$V_{GS(th)}$	-0.45		-1.5	V
						V
Gate Leakage Current		I _{GSS}			±100	nA
$(V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V})$						
Zero Gate Voltage Drain Current						
$(V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V})$		I _{DSS}			-1	μ A
$(V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C})$					-10	
On-State Drain Current						
$(V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{V})$		$I_{D(on)}$	-6			Α
$(V_{DS} \le -5 \text{ V}, V_{GS} = -2.5 \text{V})$			-3			
Drain-Source On-Resistance	Resistance					
$(V_{GS} = -4.5 \text{ V}, I_D = -2.8 \text{A})$		R _{DS(on)}		0.105	0.13	Ω
$(V_{GS} = -2.5 \text{ V}, I_D = -2.0 \text{A})$				0.145	0.19	
Forward Transconductance ($V_{DS} = -5 \text{ V}$, $I_D = -2.8 \text{V}$)		g _{FS}		6.5		S
Diode Forward Voltage (I _S =-1.6A,V _{GS} =0V)		V_{SD}		-0.8	-1.2	V
Dynamic	<u></u>	.		•	1	
Input Capacitance	$(V_{DS} = -6 \text{ V}, V_{GS} = -0 \text{V},$ f = 1.0 MHz)	C _{iss}		415		_
Output Capacitance		C _{oss}		223		pF
Reverse Transfer Capacitance		C _{rss}		87		
Turn-On Time	$I_D = -1.0 \text{ A,V}_{GEN} = -4.5 \text{ V,}$	$t_{d(on)}$		13	25	ns
Turn-On Time		tr		36	60	
Turn-Off Time		$t_{d(off)}$		42	70	
Turn-On Time	I//G = 022)	tf		34	60	
Total Gate Charge	0/ - 0// - 201	Q_g		5.8	10	
Gate-Source Charge	$(V_{DS} = -6 \text{ V}, I_D = -2.8 \text{ A},$	Q_gs		0.85		nC
Gate-Drain Charge	V _{GS} =-4.5V)	Q_{gd}		1.7		

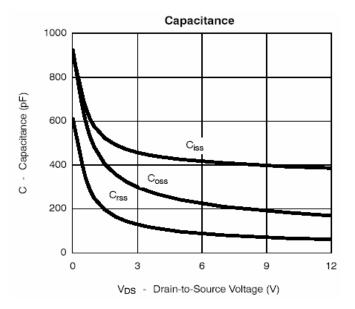


TYPICAL CHARACTERISTICS



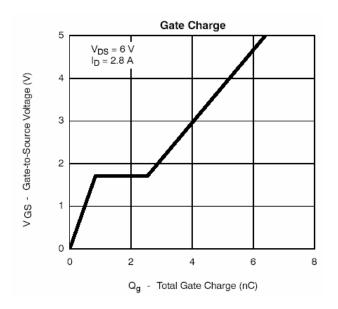


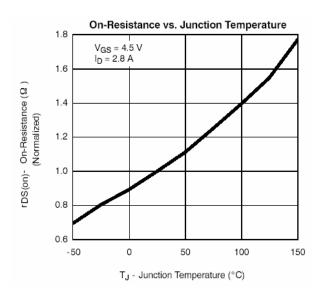


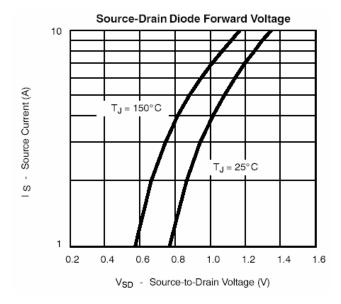


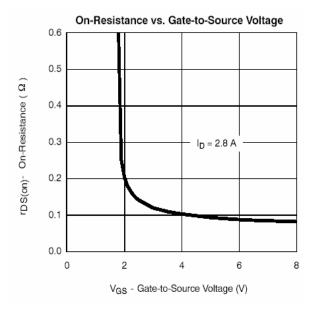


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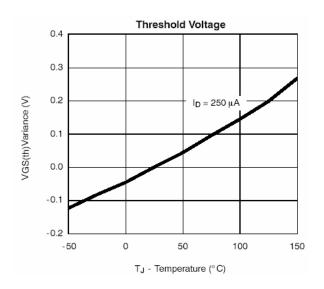


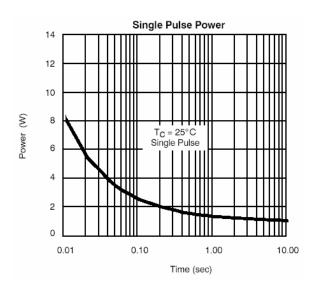


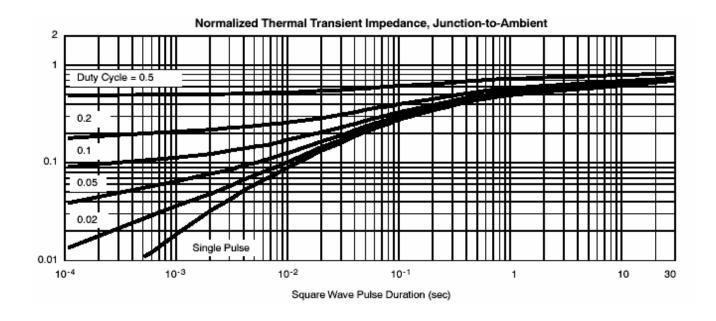




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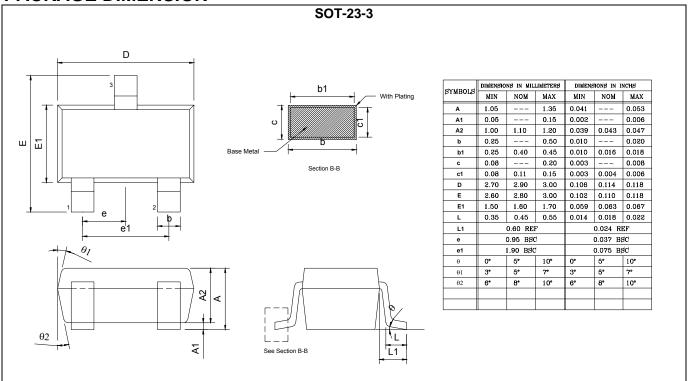








PACKAGE DIMENSION





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